



Behavioral Synthesis and Component Reuse with VHDL

Ahmed Amine Jerraya, Hong Ding, Polen Kission, Maher Rahmouni

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Improvement in the quality of integrated circuit designs and a designer's productivity can be achieved by a combination of two factors:

- Using more structured design methodologies for extensive reuse of existing components and subsystems. It seems that 70% of new designs correspond to existing components that cannot be reused because of a lack of methodologies and tools.
- Providing higher level design tools allowing to start from a higher level of abstraction. After the success and the widespread acceptance of logic and RTL synthesis, the next step is behavioral synthesis, commonly called architectural or high-level synthesis.

Behavioral Synthesis and Component Reuse with VHDL provides methods and techniques for VHDL based behavioral synthesis and component reuse. The goal is to develop VHDL modeling strategies for emerging behavioral synthesis tools. Special attention is given to structured and modular design methods allowing hierarchical behavioral specification and design reuse. The goal of this book is not to discuss behavioral synthesis in general or to discuss a specific tool but to describe the specific issues related to behavioral synthesis of VHDL description.

This book targets designers who have to use behavioral synthesis tools or who wish to discover the real possibilities of this emerging technology. The book will also be of interest to teachers and students interested to learn or to teach VHDL based behavioral synthesis.

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